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1. Process for addressing cells arranged as a matrix array, each cell being situated at the intersection of a line and a column, the array having line inputs and column inputs for displaying grey levels defined by video words making up a digital video signal and defining an image, the column inputs each receiving a control word for this column corresponding to the video word relating, for this column, to an addressed line, this word being composed of n bits transmitted sequentially, each sequence corresponding to a sub-scan, each bit triggering or not, according to its state, the illumination of the cell of the addressed line and of the column receiving the control word, for a time proportional to the weight of this bit in the word, characterized in that a different coding of the column control words is performed depending on whether the word relates to an even or odd line, this difference consisting in the fact that at least m successive bits of specified ranks, m being between 2 and n , have different weights from one control word to the other, the sum of the weights of these bits remaining identical from one control word to the other, so as to obtain writing instants which are substantially different from one line to the next.

2. Process according to Claim 1, characterized in that writing is simultaneous on two successive lines for at least the first bit of the m successive bits of a control word relating to one of the two lines.

3. Process according to Claim 1 or 2, characterized in that at least two successive lines are selected simultaneously for at least one of the bits of a specified rank, which has an identical weight from one control word to the other.

4. Process according to one of the preceding claims, characterized in that at least one of the bits of a specified rank, which has an identical weight from one control word to the other, is used to code a

partial value of luminance common to two successive lines and in that writing is simultaneous on these lines for this bit of the control word relating to one of the two lines.

5. Process according to Claim 1, characterized in
that it is implemented for a limited number of lines of
the matrix array, these lines corresponding to the
zones of the image defined by the video signal having
strong vertical transitions, the other zones utilizing
sub-scans corresponding to an addressing process for
which the column control words all have the identical
weights from one line to the other.

6. Process according to Claim 1, characterized in
that it is implemented for images having strong
vertical transitions, the other images utilizing an
addressing process for which the column control words
all have the identical weights from one line to the
other.

7. Process according to Claim 1, characterized in
that the switchover from the first addressing process
comprising n sub-scans to a second addressing process
comprising a larger number of sub-scans and for which
the column control words have a larger number of bits
having identical weights from one line to the other is
performed by replacing the selection of a line 1 while
writing a bit of different weight on the line 1, in the
first process, by the selection of the line 1 and of
the immediately preceding or immediately following line
for a simultaneous writing on these two lines, in the
second process.

8. Process according to Claim 1, characterized in
that the value of m or that of the weights
corresponding to these m bits is dependent on the
vertical resolution of the image.

9. Process according to one of the preceding
claims, characterized in that the cells are cells of a
plasma panel and in that the selection causes the
illumination of the cell.

10. Process according to one of the preceding claims, characterized in that the cells are micromirrors of a micromirror circuit.

11. Device for implementing the process according to Claim 1 comprising a video processing circuit (19) for processing the video data received, a correspondence memory (21) for transcoding this data, a video memory (22) for storing the transcoded data, the video memory being linked to column supply circuits (23) for controlling the column addressing of the plasma panel on the basis of column control words, a control circuit (24) for the line supply circuits (25) linked to the video processing circuit so as to select the lines, characterized in that the video processing and transcoding circuits perform a different coding of the column control words depending on whether the word relates to an even or odd line, this difference consisting in the fact that at least m successive bits of specified ranks from among the bits to be transmitted, m being between 2 and n , have different weights from one control word to the other, the sum of the weights of these bits remaining identical from one control word to the other, so as to obtain writing instants which are substantially different from one line to the next.

12. Device according to Claim 11, characterized in that the circuit for controlling the line supply circuits simultaneously selects two consecutive lines during the transmission by the column supply circuits of the first bit of the successive bits of a control word relating to one of the two lines.

13. Device according to Claim 11, characterized in that it also comprises a selection circuit (20) receiving the video data so as to select a coding of the column control words corresponding to an addressing according to n sub-scans or to an addressing corresponding to a larger number of sub-scans, as a function of the variations in luminance from one line to the other in an image or an image part.

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